

# NTMFS4707N

## Power MOSFET

30 V, 17 A, Single N-Channel,  
SOIC-8 Flat Lead

### Features

- Fast Switching Times
- Low Gate Charge
- Low  $R_{DS(on)}$
- Low Inductance SOIC-8 Package
- These are Pb-Free Devices

### Applications

- Notebooks, Graphics Cards
- DC-DC Converters
- Synchronous Rectification

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	10.2	A
			$T_A = 85^\circ\text{C}$	7.4	
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$	17		
Power Dissipation (Note 1)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	2.3	W
				$t \leq 10$ s	
Continuous Drain Current (Note 2)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	6.9	A
			$T_A = 85^\circ\text{C}$	4.9	
Power Dissipation (Note 2)		$P_D$	$T_A = 25^\circ\text{C}$	1.0	W
Pulsed Drain Current	$t_p \leq 10$ $\mu\text{s}$	$I_{DM}$	51	A	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	6.25	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 25$ V, $V_{GS} = 10$ V, $I_{PK} = 7.0$ A, $L = 10$ mH, $R_G = 25$ $\Omega$ )		$E_{AS}$	245	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	55	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	20	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	122.5	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

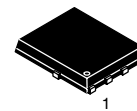
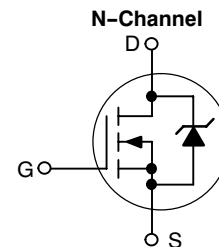
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq).



ON Semiconductor®

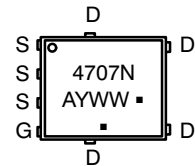
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	$I_D$ Max
30 V	10 m $\Omega$ @ 10 V	17 A
	13.5 m $\Omega$ @ 4.5 V	



SOIC-8 FLAT LEAD  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM & PIN ASSIGNMENT



4707N = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4707NT1G	SOIC-8 FL (Pb-Free)	1500 / $\bar{a}$ pe & Reel
NTMFS4707NT3G	SOIC-8 FL (Pb-Free)	5000 / $\bar{a}$ pe & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS4707N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			6.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		50	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20V			±100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		10	13	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8.0 A		13.5	17	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		20		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 24 V		735		pF
Output Capacitance	C <sub>OSS</sub>			295		
Reverse Transfer Capacitance	C <sub>RSS</sub>			80		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 10 A		7.5	15	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.1		
Gate-to-Source Charge	Q <sub>GS</sub>			2.0		
Gate-to-Drain Charge	Q <sub>GD</sub>			3.6		
Gate Resistance	R <sub>G</sub>			2.4		

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1.0 A, R <sub>G</sub> = 3.0 Ω		6.0		ns
Rise Time	t <sub>r</sub>			5.0		
Turn-Off Delay Time	t <sub>d(off)</sub>			19		
Fall Time	t <sub>f</sub>			11		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 6.25 A	T <sub>J</sub> = 25°C	0.79	1.0	V
			T <sub>J</sub> = 125°C	0.59		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 6.25 A		26		ns
Charge Time	t <sub>a</sub>			14		
Discharge Time	t <sub>b</sub>			12		
Reverse Recovery Charge	Q <sub>RR</sub>			19		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERIZATIONS

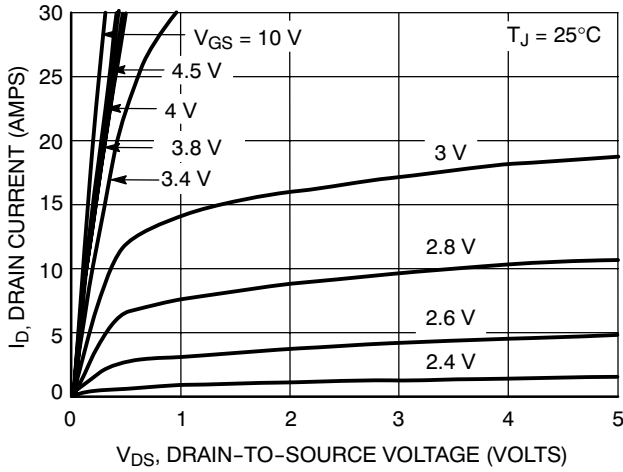


Figure 1. On-Region Characteristics

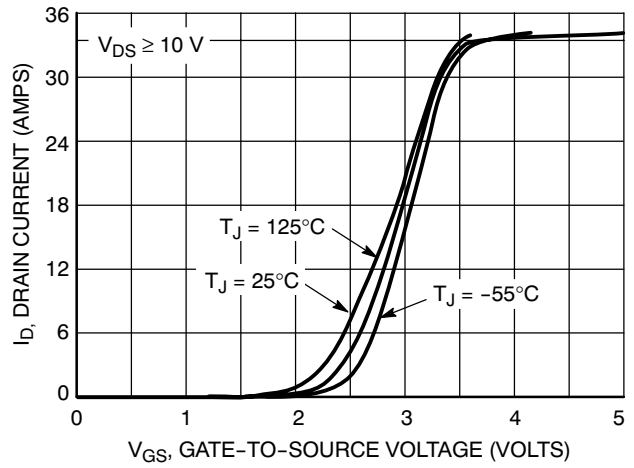


Figure 2. Transfer Characteristics

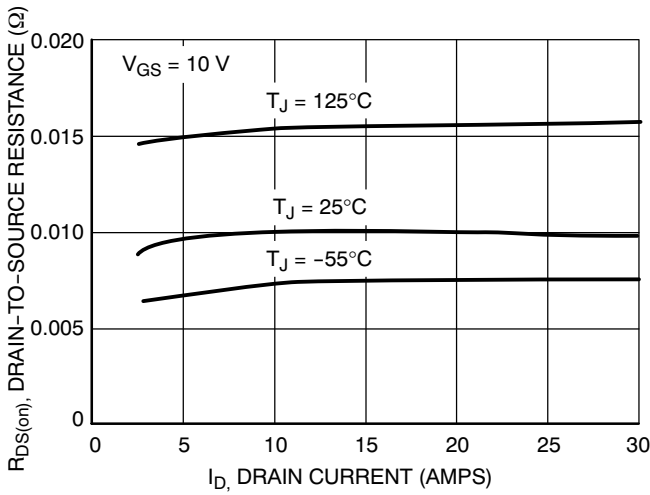


Figure 3. On-Resistance vs. Drain Current and Temperature

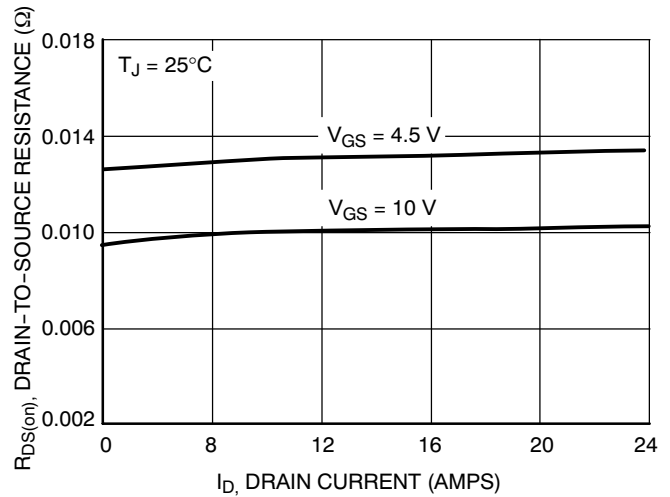


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

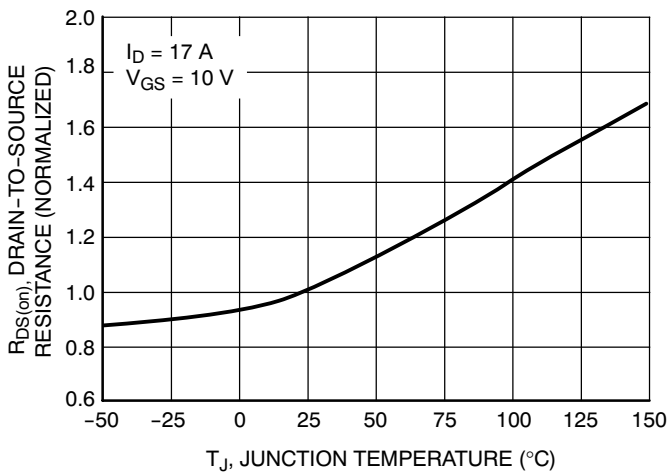


Figure 5. On-Resistance Variation with Temperature

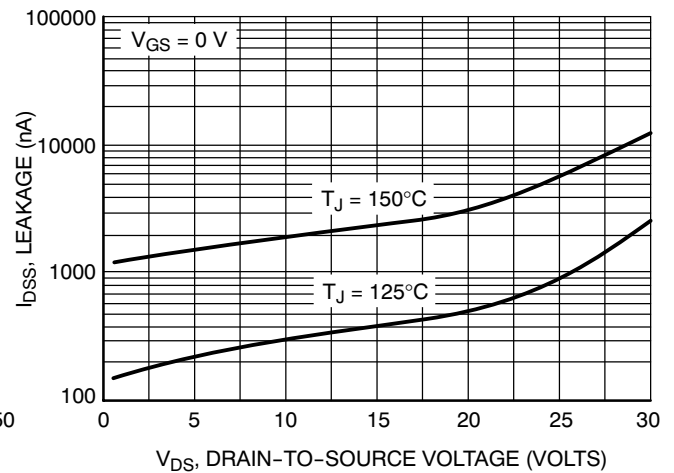


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERIZATIONS

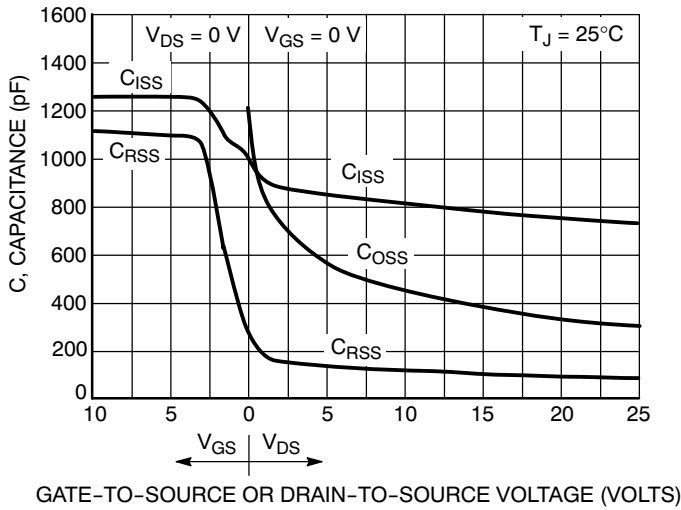


Figure 7. Capacitance Variation

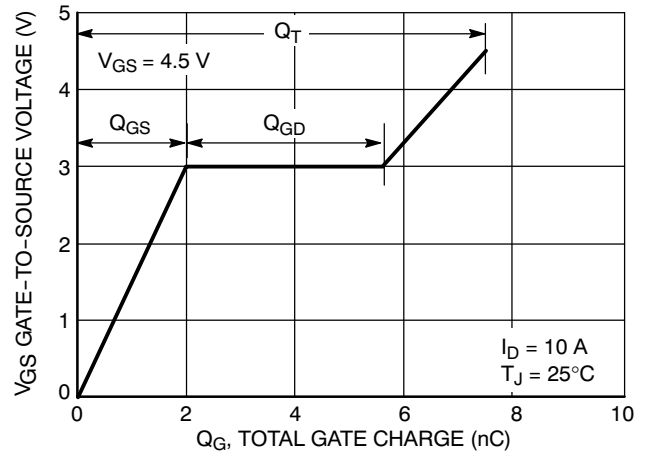


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

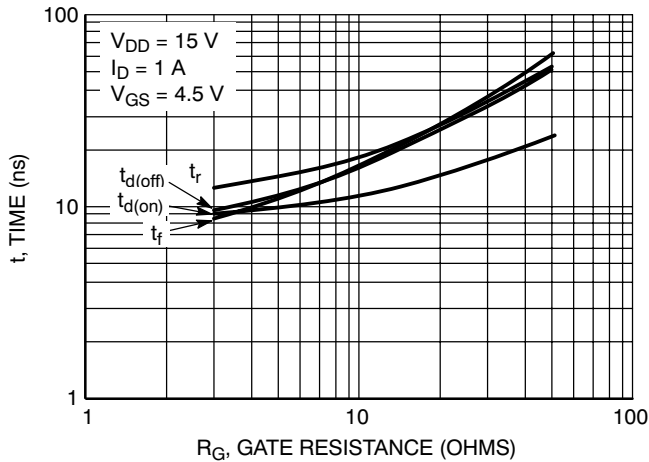


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

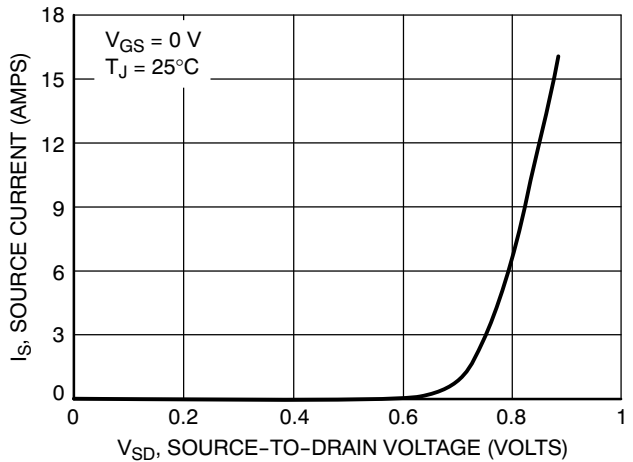


Figure 10. Diode Forward Voltage vs. Current

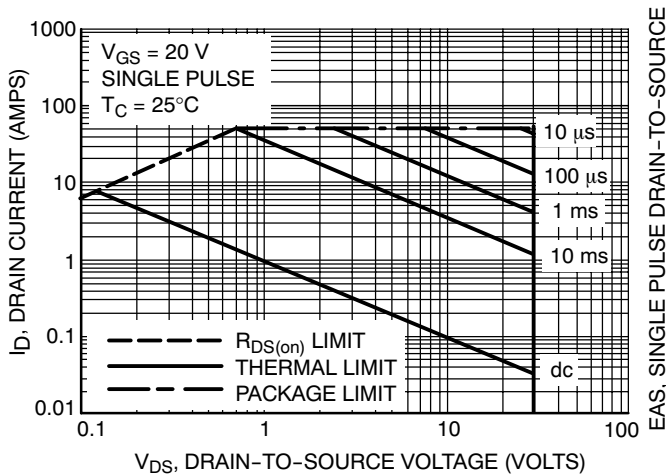


Figure 11. Maximum Rated Forward Biased Safe Operating Area

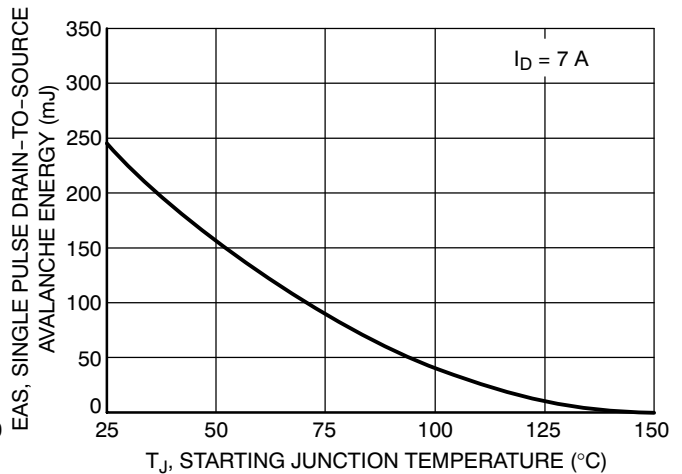
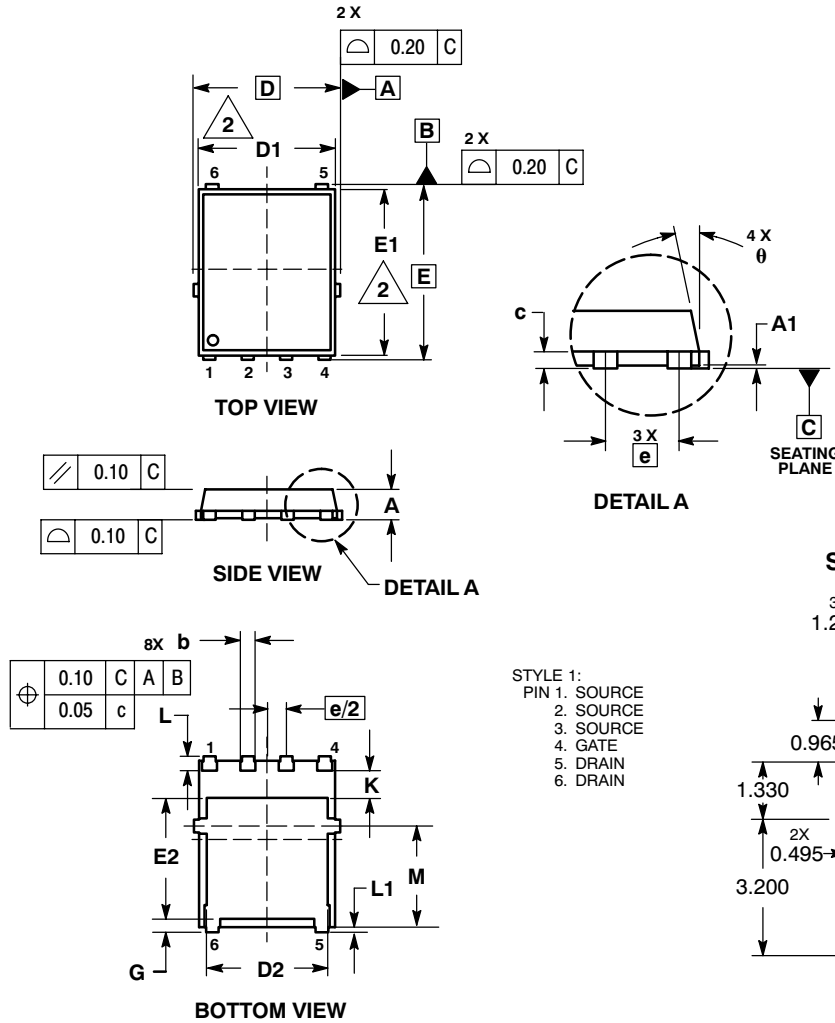


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# NTMFS4707N

## 3. PACKAGE DIMENSIONS

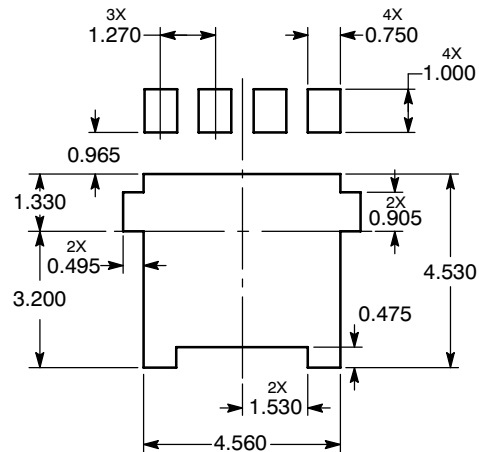
DFN6 5x6, 1.27P (SO8 FL)  
CASE 488AA-01  
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	---	---
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

### SOLDERING FOOTPRINT\*



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN  
6. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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